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Design Methodology of a Three-Phase Dual Active Bridge Converter for Low Voltage Direct Current Applications

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Abstract

The practical design methodology of a three-phase dual active bridge (3ph-DAB) converter applied to low voltage direct current (LVDC) applications is proposed by using a mathematical model based on the steady-state operation. An analysis of the small-signal model (SSM) is important for the design of a proper controller to improve the stability and dynamics of the converter. The proposed lead-lag controller for the 3ph-DAB converter is designed with a simplified SSM analysis including an equivalent series resistor (ESR) for the output capacitor. The proposed controller can compensate the effects of the ESR zero of the output capacitor in the control-to-output voltage transfer function that can cause high-frequency noises. In addition, the performance of the power converter can be improved by using a controller designed by a SSM analysis without additional cost. The accuracy of the simplified SSM including the ESR zero of the output capacitor is verified by simulation software (PSIM). The design methodology of the 3ph-DAB converter and the performance of the proposed controller are verified by experimental results obtained with a 5-kW prototype 3ph-DAB converter.

Key words: Controller design, Low voltage direct current (LVDC), Small-signal model (SSM), Three-phase DAB (3ph-DAB) converter

I. INTRODUCTION

Recently, interest in DC Microgrids (DC MGs) has increased in an effort to reduce fossil fuel consumption and improve power transmission efficiency [1]-[3]. A DC MG has many advantages over traditional AC distribution systems, such as high-power transfer efficiency and ease of connection to renewable energy sources. A multi-terminal low voltage direct current (LVDC) system has been considered to improve the flexibility and efficiency of distributed power sources [4]. A conceptual diagram of an LVDC distributed system is shown in Fig. 1. The LVDC system of the DC MG is used to distribute electric power to end users. A variety of renewable sources such as wind power, photovoltaic (PV), and energy storage system (ESS) can be easily connected to LVDC buses [5].

The LVDC converter is required for the safety of end users to convert high voltages to low voltages. A powerful candidate for a LVDC power converter is the three-phase dual active bridge (3ph-DAB) converter shown in Fig. 2. The 3ph-DAB converter includes three bridge legs on the primary and secondary sides, a coupling inductor, and a three-phase transformer. The 3ph-DAB converter has been studied for high power applications since this topology is characterized by reduced switching loss due to its zero-voltage switching (ZVS) capability and dividing the current by the phase to reduce conduction losses [6]-[8]. A mathematical model of the converter was used to propose the basic operating principle and design method [6]. Previous research on this hardware has only investigated design methods that assume ideal behavior. However, practical design methodologies that

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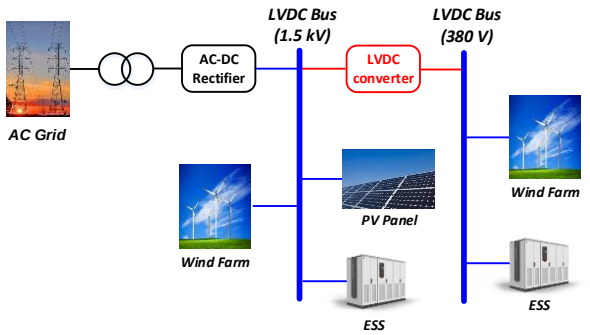


Fig. 1. Conceptual diagram of a LVDC system.

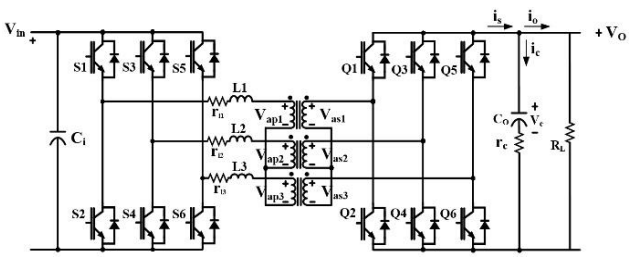


Fig. 2. Schematic of three-phase DAB converter.

consider non-ideal transformers and coupling inductances should be derived to manufacture the 3ph-DAB converters in industrial applications.

Designing a suitable controller for a power converter requires an analysis based on a small-signal model (SSM), which can improve the stability and dynamics of the converter [15]. In a previous study, a simplified SSM of a 3ph-DAB converter was introduced to design a current-balancing control algorithm for a three-phase transformer [9]. However, the simplified SSM in [9] excludes the effects of the ESR zero of the output capacitor. The ESR zero of the output capacitor in the control-to-output voltage transfer function makes the converter much weaker in terms of high-frequency noise due to reduced damping at high-frequencies. Therefore, a lead-lag controller, which can compensate the ESR zero of the output capacitor, is required in practical applications.

This paper briefly introduces the operational principle of the 3ph-DAB converter. Practical design considerations such as the effects of transformer winding types and coupling inductance will be presented in Section II. In Section III, the lead-lag controller design methodology will be proposed to compensate for the effects of the ESR zero of the output capacitor based on a simplified SSM of the converter including the ESR zero of the output capacitor. Finally, the proposed lead-lag controller will be verified with experimental results using a 5-kW prototype 3ph-DAB converter.

II. Design Methodology

In high power applications, the 3ph-DAB converter can be a good candidate for a competent topology. This topology has

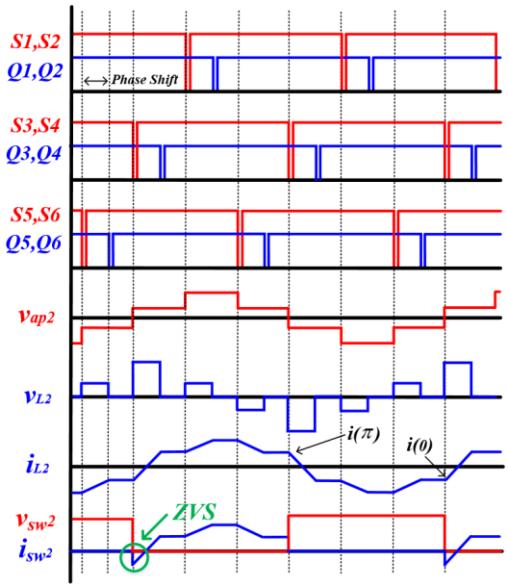


Fig. 3. Theoretical waveforms of a three-phase DAB converter in the forward power flow.

the advantages of a relatively simple bi-directional control algorithm and a symmetric structure. In addition, the 3ph-DAB converter can achieve ZVS of the power switch without auxiliary components, which can improve the overall power conversion efficiency.

A. Operational Principle

Theoretical waveforms of the 3ph-DAB converter under a forward power flow are shown in Fig. 3. The converter has a phase difference of 120° in each phase. Its operational principle is similar to that of a single-phase DAB converter using single-phase shift modulation between the primary and secondary side. There are two operating modes depending on the current direction. Power is transmitted from the primary side to the secondary side when the phase of the primary side leads to that of the secondary side, and vice versa. The coupling inductance combined with the series inductance and the leakage inductance of the transformer is used as the power transfer component in the 3ph-DAB converter.

B. Y-Y and Y-⊿ Transformer

3-phase transformers should be selected by considering the characteristics of the winding types. There are two types of windings in three-phase converter [10]: 1) Y-Y windings; and 2) Y-Δ windings. The turn ratio for each of the windings is different. Thus, the Y-Y and the Y-Δ windings are 1:1 and 1: $\sqrt{3}$ n, respectively. Due to the turn ratio, the Y-Δ connection is advantageous for high voltage applications. In high-power applications, a high leakage inductance due to a lot of turn number leads to a lot of transformer losses. On the other hand, the Y-Y connection is advantageous for maintaining the current balance of each leg since it has the same structure on the primary and secondary sides.

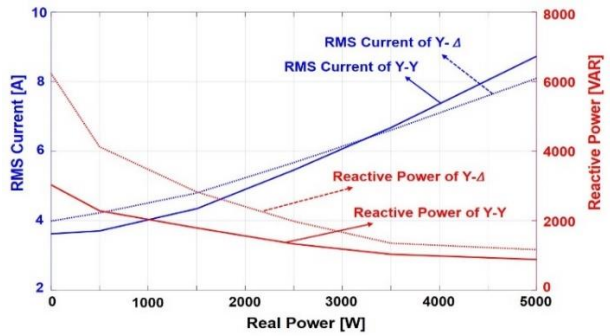


Fig. 4. Comparison of the RMS current and reactive power between the Y-Y windings and Y-Δ windings.

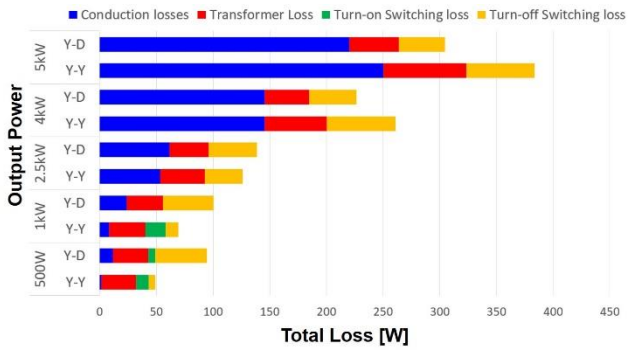


Fig. 5. Loss comparisons between the Y-Y and Y-Δ connections.

In order to determine the desired winding type in a 3-phase converter, the winding types should be compared with each other in terms of the RMS current and reactive power while considering the power conversion efficiency. The RMS current of the Y-Y windings and Y-Δ windings can be obtained as follows:

$$I_{Y-Y\_RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_{Y-Y}(t)d\theta)^2} = \frac{\sqrt{V_i^2\left(5(n-1)^2\pi^2 + 54n\pi\varphi^2 - 27n\varphi^3\right)}}{9\sqrt{3}\omega L} \quad (1)$$

$$I_{Y-\Delta\_RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_{Y-\Delta}(t)d\theta)^2} = \frac{\sqrt{V_iV_o\left(5\pi^2(1-3n+3n^2) - 27n\pi\varphi + 81n\pi\varphi^3\right)}}{9\sqrt{3}\omega L} \quad (2)$$

where V_i and V_o are the input and output voltages, L is the coupling inductance, ω is the switching angular frequency, n is the turn ratio of the transformer, and φ is the phase-shift angle. Fig. 4 shows a comparison of the tendency of the RMS currents and reactive power according to an increase in the output power. In Fig. 4, the blue line and dotted-blue line represent the RMS current of the Y-Y windings and Y-Δ windings, respectively. The RMS current of the Y-Δ windings is higher than that of the Y-Y windings under light load conditions. However, RMS current of the Y-Y windings is higher than that of the Y-Δ winding under medium or higher load conditions.

A comparison of the reactive power versus an increase of the output power is shown in Fig. 4. In Fig. 4, the red line and dotted red line indicate the reactive powers of the Y-Y windings and Y-Δ windings, respectively. The reactive power of the Y-Δ windings is higher than that of the Y-Y windings since the Y-Δ windings have a 30° phase delay due to its structure. This natural feature of the Y-Δ windings can be explained by the transmitted power of the 3ph-DAB converter when the Y-Δ windings are applied as follow:

$$P_{Y-\Delta}(\varphi) = \frac{1}{2\pi}\int_0^{2\pi} i_a(t)v_a(t)dt = \frac{nV_iV_o}{\omega L}(\varphi - \frac{\pi}{6}), \left(0 \le \varphi \le \frac{\pi}{3}\right) \quad (3)$$

From (3), the direction of the transmitted power is reversed until the phase is shifted to 30° in the Y-Δ windings, which implies a 30° phase delay. This means that the power can be transmitted from the primary side to the secondary side after the phase is shifted to 30° in the Y-Δ windings. As shown in Fig. 5, although the Y-Y windings have a higher power loss under heavy load conditions, the power efficiency is high under most of the load condition, especially under light load conditions. Due to the design considerations for the power margin, the normalized phase-shift cannot reach 1, which can reduce the conduction loss under heavy load conditions. In addition, the Y-Y connection can reduce the current imbalance of each leg since the transformer structure is the same on both sides. Therefore, the Y-Y windings was chosen as the transformer structure of the 3ph-DAB converter.

The number of windings of the transformer can be selected from the voltage waveform of the transformer in accordance with Faraday's law as shown in Fig. 3. The number of windings is proportional to the leakage inductance, which causes the transformer losses. Therefore, the minimum number of windings is required [11], [12]. The minimum number of primary winding can be calculated as follows:

$$N_{p,\min} = \frac{D(\frac{1}{9}V_i + \frac{2}{9}V_i + \frac{1}{9}V_i)}{4B_{\max}A_e f_s} \quad (4)$$

where D is the duty ratio, B_{max} is the maximum flux density, A_e is the effective cross-sectional area of the transformer's core, f_s is the switching frequency, and V_i is the input voltage.

C. Design of the Proper Coupling Inductance

The design of the coupling inductance is important for the proper operation of the 3ph-DAB converter [6]. The average current can be obtained by integrating the inductor current during half of a switching period as shown in Fig. 3. The output power of the 3ph-DAB converter using the Y-Y windings can be expressed as (5).

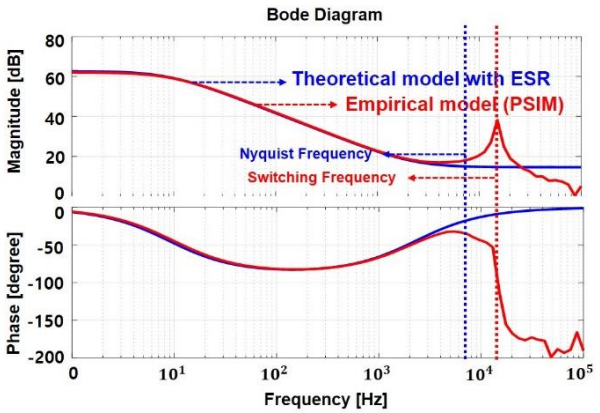


Fig. 6. Control-to-output voltage transfer function of a three-phase DAB converter from 0 Hz to 100 kHz.

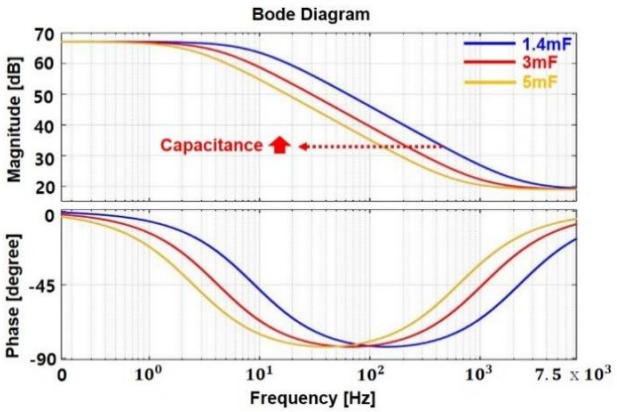


Fig. 7. Magnitude and phase Bode plots of a transfer function according to output capacitance increments.

$$P_{Y-Y}(\varphi)=\frac{1}{2\pi}\int_0^{2\pi} i_a(t)v_a(t)dt=\frac{nV_iV_o}{\omega L}\varphi\left(\frac{2}{3}-\frac{\varphi}{2\pi}\right),\ \left(0\le\varphi\le\frac{\pi}{3}\right) \quad (5)$$

The coupling inductance can be calculated by (5). A 20% margin of the output power is generally considered to design the coupling inductance [16], [17]. The coupling inductance is related to the losses. If the coupling inductance is too small, high switching losses occur under the light load condition. In addition, the current variations are very sensitive resulting in imbalance-leg currents. However, the use of a calculated coupling inductance based on the maximum power without a margin increases the RMS current. Therefore, when choosing the coupling inductance, a balance between the switching loss and the conduction loss should be considered.

III. Controller Design

A. Analysis of the Small-Signal Model

A SSM analysis is important in the design of a controller to improve the stability and dynamics of the converter. The simplified SSM of a 3ph-DAB converter was first analyzed to reduce the imbalance of the winding current for a transformer [9]. However, the ESR zero of the output capacitor was not considered to derive the control-to-output voltage transfer function in [9]. A simplified model considering the ESR zero of the output capacitor can be derived by using an existing simplified model. It is assumed that the 3-phase voltage and current are well balanced and that the power flows in the forward direction. A fundamental waveform of the 3ph-DAB converter is shown in Fig. 3.

The capacitor voltage is only used as a state variable to obtain a simplified SSM with the ESR zero of the output capacitor. Using Fig. 2 and Fig. 3, the voltage differential equations can be expressed as follows:

$$V_o=V_c-r_cC_o\frac{dV_c}{dt} \quad (6)$$

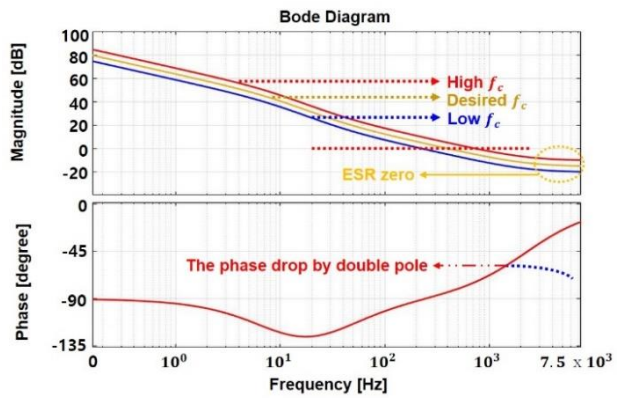


Fig. 8. Closed-loop gain with a PI controller.

$$\frac{dV_c}{dt}=\frac{i_s}{C_o\left(1+\frac{r_c}{R_L}\right)}-\frac{V_c}{R_LC_o\left(1+\frac{r_c}{R_L}\right)} \quad (7)$$

where V_c is the capacitor voltage, i_s is the secondary current, C_o is the output capacitor, r_c is the equivalent series resistor of the output capacitor, and R_L is the output resistor. The secondary current is divided into two modes and the detailed derivation procedure was presented in [9]. In the derivation process, it is assumed that the output voltage is almost equal to the capacitor voltage, $V_o \approx V_c$.

The control-to-output voltage transfer function with the ESR zero of the output capacitor is expressed as follows:

$$\frac{\Delta\tilde{V}_o}{\Delta\tilde{\varphi}}(s)=\frac{R_LV_i\left(\frac{2}{3}-\frac{\varphi}{\pi}\right)}{\omega L}\cdot\frac{r_cC_os+1}{(R_L+r_c)C_os+1}=k_{vd}\frac{\left(\frac{s}{\omega_{vd,z}}+1\right)}{\left(\frac{s}{\omega_{vd,p}}+1\right)} \quad (8)$$

$$k_{vd}=\frac{R_LV_i\left(\frac{2}{3}-\frac{\varphi}{\pi}\right)}{\omega L},\ \omega_{vd,p}=\frac{1}{(R_L+r_c)C_o},\ \omega_{vd,z}=\frac{1}{r_cC_o}$$

where V_i is the input voltage, s is the Laplace operator, $k_{vd,z}$ is the gain of the transfer function, $\omega_{vd,z}$ is the single-zero, and $\omega_{vd,p}$ is the single-pole. A comparison of the control-to-

TABLE I
DESIGN SPECIFICATIONS

Output Power, P_o	5 kW
Input Voltage, V_i	500 V
Output Voltage, V_o	252 V
Switching Frequency, f_s	15 kHz
Output Capacitance, C_o	1.4 mF
Phase Shift, φ	$0^\circ < \varphi < 56^\circ$
Coupling Inductance, L	240 uH
Turn ratio, N_2/N_1	0.5
Turn Number, N_1	20 turns
ESR of Capacitor, r_c	0.05 Ω
Output Resistor, R_L	12.7 Ω

output voltage transfer function between the theoretical model and the empirical model is shown in Fig. 6. The blue line shows a Bode-plot of the theoretical model using (8) and TABLE I. The red line shows empirical data using simulation software (PSIM) with the same parameters. The model error of the simplified model in the high-frequency region is caused by inductor dynamics since the simplified model considers only the output capacitor with the ESR zero as the state variable. However, the simplified model is accurate to show the effect of the ESR zero of the output capacitor within the Nyquist frequency, which is the blue line shown in Fig. 6. The model error is not significant to design its controller because all of the dynamics of the converter are discussed within the Nyquist frequency. The 3ph-DAB converter has a single pole located in the low-frequency region and an ESR zero of the output capacitor located in the high-frequency region.

The magnitude and phase change of the control-to-output voltage transfer function with increments of the output capacitance are shown in Fig. 7. For high-power applications, the output capacitance should be increased to reduce output voltage ripple and to suppress power fluctuations. However, a higher output capacitance makes the converter dynamics slower than the case of a lower output capacitance. The crossover frequency moves to the low-frequency region as the output capacitance increases. A low crossover frequency improves the stability. However, it makes the transient performance poor. If the ESR zero of the output capacitor is not compensated, the magnitude of the control-to-output voltage transfer function shows a 0 dB/decade slope after the ESR zero. This reduced damping in the high-frequency region makes the system weaker against disturbances and noise. Therefore, the ESR zero of the output capacitor should be compensated by the desired lead-lag controller.

B. Controller Design

A PI controller is typically used for the 3ph-DAB converter. However, they cannot compensate for the output

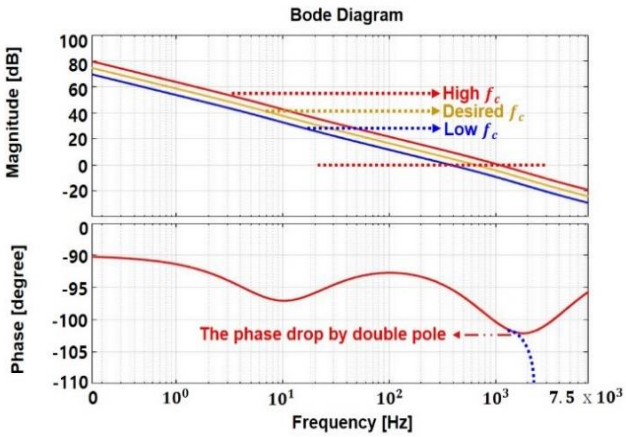


Fig. 9. Closed-loop gain with a 2P1Z controller.

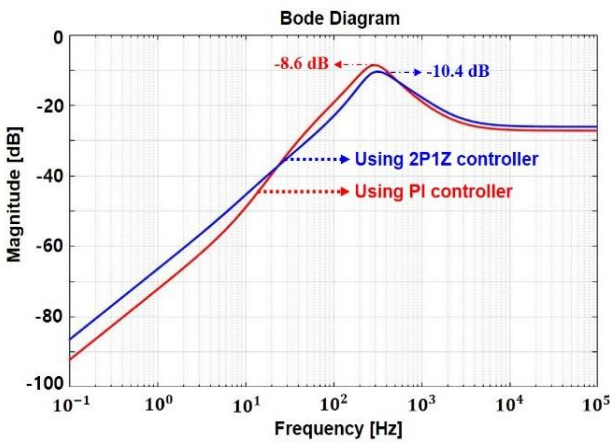


Fig. 10. Comparison of the output impedances using a PI and a 2P1Z controller in the s-domain.

capacitor's ESR zero in the control-to-output voltage transfer function. A 2-pole 1-zero (2P1Z) controller with an additional pole, which can compensate the ESR zero, is presented and compared with the PI controller. Each controller was designed by using the k-factor approach [13-14]. The transfer function of the PI controller can be expressed as follows:

$$G_{c,Pi}(s) = K_{pi}\frac{\left(1+\dfrac{s}{\omega_{pi,z}}\right)}{s} \tag{9}$$

where k_{pi} is the gain of the PI controller and $\omega_{pi,z}$ is the single zero. The PI controller consists of a pole at the origin and a single zero. The closed-loop gain of the converter with a PI controller is shown in Fig. 8. The red line shows the high crossover frequency case, which can be oscillated by external disturbances and noises. As shown in Fig. 6, the control-to-output voltage transfer function of the empirical model has a phase-drop due to the double pole at the switching frequency. Therefore, to guarantee stability, the crossover frequency should be less than 1 kHz. The blue line shows the low crossover frequency case, which can show slow dynamics

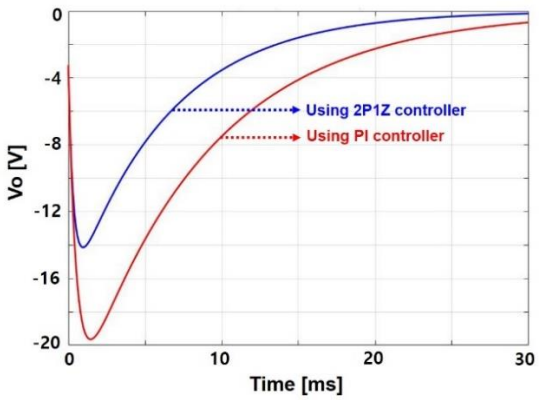


Fig. 11. Comparison of the transient performance using a PI and a 2P1Z controller in the time-domain.

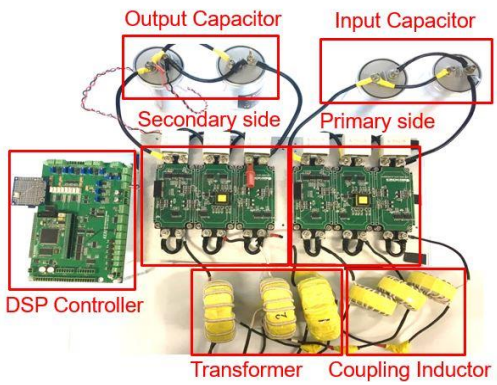


Fig. 12. 5 kW prototype of the three-phase DAB converter.

and a high overshoot. Therefore, the yellow line design is selected to achieve a balance between the performance and stable operation of the PI controller. In this design, the crossover frequency is set to 400 Hz and the single zero is placed at 35 Hz.

The ESR zero of the output capacitor has a magnitude of 0 dB/decade slope in the high-frequency range, which makes the converter sensitive to high-frequency disturbances and noise. For the desired performance of the feedback control, the controller is required to compensate for the poles and zeros of the loop gain of the converter, which should have a -20 dB/decade slope of the Bode plot's magnitude in all of the frequency regions [15].

The transfer function of the 2P1Z controller can be expressed as follows:

$$G_{c,2p1z}(s) = K_{2p1z}\frac{1+\dfrac{s}{\omega_{2p1z,z}}}{s\left(1+\dfrac{s}{\omega_{2p1z,p}}\right)} \tag{10}$$

where k_{2p1z} is the gain of the 2P1Z controller, and $\omega_{2p1z,z}$ and $\omega_{2p1z,p}$ are the single zero and the pole of the controller, respectively. Unlike the PI controller, the 2P1Z controller consists of a pole at the origin, and a single zero and a single pole, which can compensate the ESR zero of the output capacitor. The closed-loop gain of the 2P1Z controller is shown in Fig. 9. The crossover frequency is divided into three cases similar to the PI controller. The red line represents the case of a high crossover frequency, which can be affected by an external disturbance with a phase collapse. The blue line indicates the low crossover frequency case, which has slow dynamics and a high overshoot in the transient response. Therefore, the yellow line is chosen as the desired control point. The crossover frequency is selected at 650 Hz. The pole and zero frequencies are located at 1.485 kHz and 11.37 Hz, respectively. The slope of the Bode plot's magnitude has a -20 dB /decade due to the compensation of the ESR zero of the output capacitor by the single pole of the 2P1Z controller.

TABLE II
PERFORMANCE COMPARISON

	Undershoot		Settling time	
	Theoretical	Experiment	Theoretical	Experiment
PI	360.4 *V*	362 *V*	13.3 *msec*	15 *msec*
2P1Z	365.8 *V*	366 *V*	7.71 *msec*	9 *msec*

C. Output Impedance Analysis

The load current-to-output voltage transfer function under the open-loop condition can be expressed as follows [13]:

$$Z_p(s) = k_p\frac{\left(1+\dfrac{s}{\omega_{z1}}\right)\left(1+\dfrac{s}{\omega_{z2}}\right)}{\left(1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}\right)} \tag{11}$$

$$k_p = (r_l R_L)/(r_l + R_L), \omega_{z1} = r_l/L, \omega_{z2} = 1/r_c C_o$$

$$\omega_o = \frac{1}{\sqrt{LC_o}}\sqrt{\frac{r_l + R_L}{r_c + R_L}},\ Q = \sqrt{\frac{L}{C}}\frac{1}{r_c + r_l}$$

where k_p is the gain of the transfer function, ω_{z1} and ω_{z2} are the single zero, ω_o is the double pole, Q is the quality factor, and r_l is the ESR of the inductance. Using (11), the output impedance for each of the controllers can be expressed as follows:

$$Z_{o,PI}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_o(s)} = \frac{Z_p(s)}{1+T_{m,PI}(s)}$$

$$Z_{o,2P1Z}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_o(s)} = \frac{Z_p(s)}{1+T_{m,2P1Z}(s)} \tag{12}$$

where $Z_{o,PI}$ and $Z_{o,2P1Z}$ are the output impedance of each controller, and $T_{m,PI}$ and $T_{m,2P1Z}$ are the closed-loop gain of each controller. Each output impedance in the s-domain is shown in Fig. 10, where the blue line is the output impedance using the 2P1Z controller and the red line is that of the PI controller. Since the peak value of the 2P1Z controller is smaller than that of the PI controller, the 2P1Z controller can further suppress disturbance.

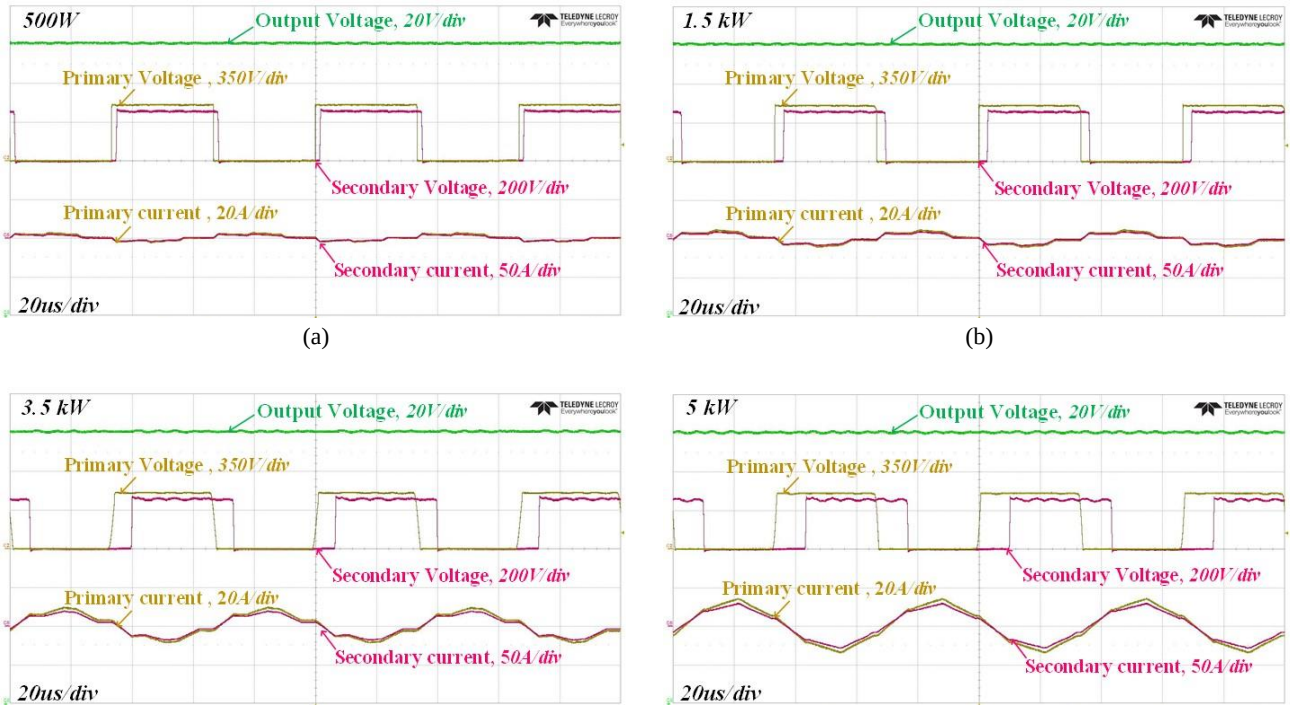


Fig. 13. Experimental waveforms during steady-state operation: (a) 500 W; (b) 1.5 kW; (c) 3.5 kW; (d) 5 kW.

The theoretical transient performance for each of the controllers in the time-domain with changes in step load change from 7 A to 14 A is shown in Fig. 11, where the red line represents the output voltage using the PI controller and the blue line represents the output voltage using the 2P1Z controller. The output voltage for each of the controllers in the time-domain can be expressed theoretically as follows:

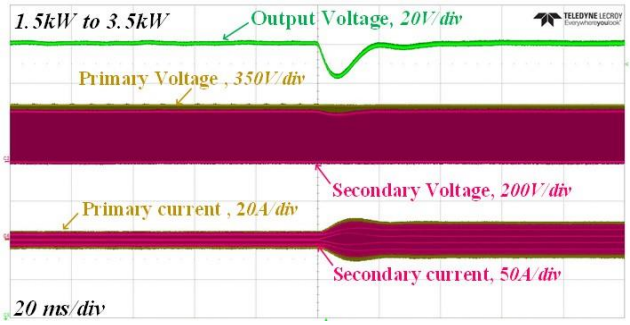
$$V_{o,PI}(t) = \mathcal{L}^{-1}\left\{\frac{I_{step}}{s} Z_{o,PI}\right\} = 21.6851e^{-1947t} - 24.9184e^{-120.2t}$$

$$V_{o,2P1Z}(t) = \mathcal{L}^{-1}\left\{\frac{I_{step}}{s} Z_{o,2P1Z}\right\} = 13.9202e^{-2978t} - 17.42e^{-159.6t} \quad (13)$$

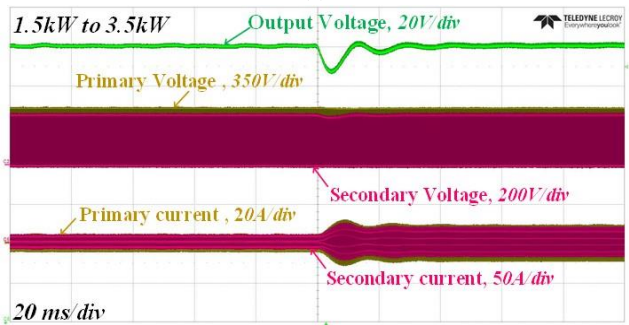
where $V_{o,2p1z}$ is the output voltage using the 2P1Z controller, I_{step} is set to 7 A, and $V_{o,pi}$ is the output voltage using the PI controller in the time-domain. This can be obtained by using the Inverse Laplace Transform from (8), (9), (10) and TABLE I. In (12), the undershoot using the 2P1Z controller is about -14.2 V, and the PI controller is expected to be about -19.6 V. In addition, the settling time of the 2P1Z controller is expected to be faster than that of the PI controller. The settling time of the 2P1Z controller is expected to be within 7.71 msec, and that of the PI controller is expected to be within 13.3 msec. A comparison of the undershoot and settling time for each of the controllers is presented in TABLE II. It can be seen that the transient response of the 2P1Z controller is faster than that of the PI controller. The transient performance expected by the theoretical analysis will be verified with experimental results in the next section.

IV. Experimental Results

A 5-kW prototype 3ph-DAB converter is shown in Fig. 12. The 3ph-DAB converter consists of three IGBT modules, three inductors, input and output capacitors, a three-phase transformer based on a nanocrystalline toroidal core, TC-805024-1, and a DSP control board. The detail specifications of the converter are shown in Table I. The inductance and the turn number of the transformer can be obtained from (4) and (5). Experimental waveforms during steady-state operation using the proposed 2P1Z controller are shown in Fig. 13. The phase between the primary and the secondary side is shifted from 0° to 56° according to load variations. The larger load induces a larger phase shift, and vice versa. The output voltage is well regulated to 252 V. The RMS inductor current at the full load conditions is measured at around 9 *A*, which was predicted in the theoretical analysis shown in Fig. 4. A comparison of the performance between PI and 2P1Z controllers is shown in Fig. 14. The undershoot of the output voltage using a 2P1Z controller is measured at around -14 *V* under a step load change from 7 *A* to 14 *A* while that of the PI controller is measured at around -18 *V*. The settling time of the 2P1Z controller is 9 *msec* while that of the PI controller is 15*msec*. These results show improved performance in terms of the power converter's dynamics when the 2P1Z controller



(a)



(b)

Fig. 14. Comparison of the controller performance: (a) PI controller (7A→14A); (b) 2P1Z controller (7A→14A).

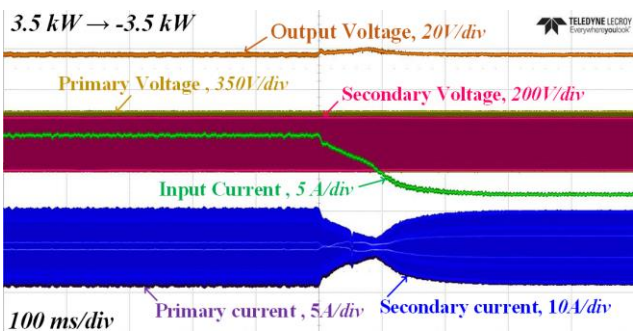


Fig. 15. Bi-directional experimental waveform (3.5 *kW* → -3.5 *kW*).

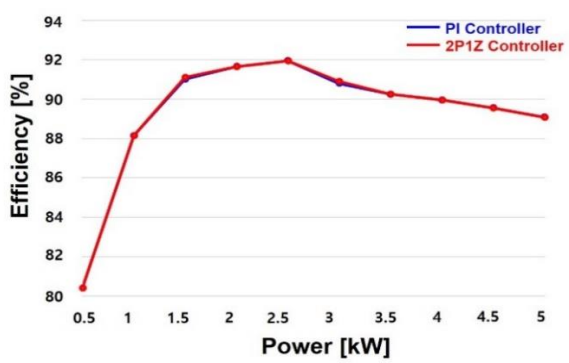


Fig. 16. Efficiency graphs of the proposed converter using a PI and a 2P1Z controller.

is applied since it has a high crossover frequency. The undershoot error between the theoretical expectation and the experimental measurement is around 0.3 %, and the settling time error is around 1.3 *msec* and 5.361 *msec* for each of the controllers. These errors were caused by model errors and unexpected impedances of the converter, power source and electric load, etc. Bi-directional experimental results using a 2P1Z controller are shown in Fig. 15. A step load change from 7A to -7A can be achieved with the same control gain. Efficiency curves with a PI controller and a 2P1Z controller are shown in Fig. 16. The efficiency is at its highest at about 92 % under the 2.5 *kW* load condition. Efficiency under the light load condition is lower than that under the full load condition since the switching loss is at its highest under the light load condition. The efficiency of the proposed converter using a 2P1Z controller is similar to that of the conventional PI controller.

V. CONCLUSIONS

A practical design methodology for a 3ph-DAB converter is proposed with a mathematical analysis. In addition, a lead-lag controller with two poles and a single zero is proposed to compensate for the effects of the ESR zero of the output capacitor based on an analysis of a simplified small-signal model considering the ESR zero of the output capacitor. Because the impact of the ESR zero of the output capacitor is increased by a high capacitance, the converter can be easily affected by disturbances if the effect of the ESR zero of the output capacitor is not properly compensated. The accuracy of the small-signal model including the ESR zero of the output capacitor is verified by using simulation results. Experimental results using a 5-kW prototype 3ph-DAB converter show that the undershoot is improved by about 4 *V* and that the settling time is 6 *msec* when using the 2P1Z controller. It is verified that the proposed 2P1Z controller has a faster dynamic performance than the conventional PI controller without any additional cost. A bi-directional test can be achieved with the same control gain. The efficiency with two controllers is almost same since this is determined by the power stage design.

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